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| APPLICATION NO.         | FILING DATE | FIRST NAMED INVENTOR  | ATTORNEY DOCKET NO. | CONFIRMATION NO.  |
|-------------------------|-------------|-----------------------|---------------------|-------------------|
| 10/605,732              | 10/22/2003  | Edward P. Maciejewski | BUR920030052US1     | 2731              |
| 28211                   | 7590        | 01/04/2005            | EXAMINER            |                   |
| FREDERICK W. GIBB, III  |             |                       |                     | KRAMSKAYA, MARINA |
| MCGINN & GIBB, PLLC     |             |                       |                     | ART UNIT          |
| 2568-A RIVA ROAD        |             |                       |                     | 2858              |
| SUITE 304               |             |                       |                     | PAPER NUMBER      |
| ANNAPOLIS, MD 21401     |             |                       |                     |                   |
| DATE MAILED: 01/04/2005 |             |                       |                     |                   |

Please find below and/or attached an Office communication concerning this application or proceeding.

|                              |                              |                    |
|------------------------------|------------------------------|--------------------|
| <b>Office Action Summary</b> | Application No.              | Applicant(s)       |
|                              | 10/605,732                   | MACIEJEWSKI ET AL. |
|                              | Examiner<br>Marina Kramskaya | Art Unit<br>2858   |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

**A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.**

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) Responsive to communication(s) filed on \_\_\_\_\_.  
 2a) This action is **FINAL**.      2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4) Claim(s) 1-29 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_ is/are allowed.  
 6) Claim(s) 1-6-8, 13-15, 20-22 and 27-29 is/are rejected.  
 7) Claim(s) 2-5, 9-12, 16-19, & 23-26 is/are objected to.  
 8) Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 26 February 2004 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) Notice of References Cited (PTO-892)  
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
 Paper No(s)/Mail Date 10/22/03.

4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date. \_\_\_\_\_.  
 5) Notice of Informal Patent Application (PTO-152)  
 6) Other: \_\_\_\_\_.

**DETAILED ACTION*****Drawings***

1. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the reference numerals, reference lines and arrows, and text in drawings are unclear. Further, in Figure 1, the ammeter 16 and connection points about the DUT 14 are indistinguishable. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.
  
2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "14" has been used to designate both the *inverter* and the *DUT*. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 6, 7, 8, 13, 14, 15, 20, 21, 22, 27, 28, & 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohkawa, US 2004/0008051 A1, in view of Mahant-Shetti et al., US 4,795,964.

As per Claims 1, 8, 15, & 22 Ohkawa discloses a semiconductor structure formed on a substrate [par. 0014] comprising:

a ring oscillator **11e** receiving a first voltage **11e-5** as a power supply, wherein said ring oscillator outputs a ring oscillator output **F<sub>0</sub>**; (FIG. 2 & 7) an inverter (**11b-1**, **11b-2**) receiving said ring oscillator output as an input **11b-12** (through the control terminal), said inverter being coupled to a device under test **11b-3** and said inverter receiving a third voltage **VDD** and a fourth voltage **GND** as power supplies (FIG. 2 & 4A),

wherein current **I<sub>ddc</sub>** drawn by said inverter provides a measurement of capacitance of said device under test **11b-3** (11b: Capacity measurement pattern area, FIG. 2 & 4A).

Further, for Claim 8, Ohkawa discloses the on-chip test device and said device under test are located on the same semiconductor chip (FIG. 1 & FIG. 2).

Further, for Claim 15, Ohkawa discloses a plurality of inverters, all isolated (FIG. 1: a plurality of 11's arranged in 31 & 32).

Further, Claim 22, is disclosed in the steps above.

Ohkawa does not disclose the ring oscillator receiving a second voltage as a power supply.

Mahant-Shetti discloses the ring oscillator receiving a second voltage  $V_{ss}$  as a power supply (FIG. 1 & 4).

Therefore, it would have been obvious to a person of ordinary skill in the art to include two voltages to power the ring oscillator as taught by Mahant-Shetti, in order to have a better controlled potential between the terminals of the oscillator.

As per Claims 6, 13, & 20 Ohkawa discloses the measuring structure as applied to Claims 1, 7, & 15 above.

Ohkawa does not disclose the measurement of capacitance of said device under test to determine the thickness of a gate oxide.

Mahant-Shetti discloses the measurement of capacitance of said device under test to determine the thickness of a gate oxide (column 5, lines 18-19).

Therefore, it would have been obvious to a person of ordinary skill in the art to measure the capacitance of said device under test to determine the

thickness of a gate oxide, as taught by Mahant-Shetti, for testing field effect transistor.

As per Claims 7, 14, 21, & 29 Ohkawa discloses the measuring structure as applied to Claims 1, 7, 15, & 22 above.

Ohkawa does not disclose the device under test comprising of a gate oxide capacitor, a gate conductor, a channel, and an interconnect.

Mahant-Shetti discloses the device under test comprising of a gate oxide capacitor (column 6, line 34), a gate conductor 74 (column 6, line 40), a channel (column 6, lines 31-32), and an interconnect (FIG. 3a).

Therefore, it would have been obvious to a person of ordinary skill in the art to test the thickness of a semiconductor with a gate oxide capacitor, a gate conductor, a channel, and an interconnect, as taught by Mahant-Shetti, because it is a commonly used structure and there is a high demand for accurate testing of the said structure.

As per Claim 27, Ohkawa discloses the measuring structure as applied to Claims 1, 7, 15, & 22 above.

Ohkawa does not disclose the DUT as a gate oxide capacitor.

Mahant-Shetti discloses the DUT as a gate oxide capacitor (column 6, line 34).

Therefore it would have been obvious to a person of ordinary skill in the art to test a gate oxide capacitor, as taught by Mahant-Shetti, for testing field effect transistor.

As per Claim 28, Ohkawa and Mahant-Shetti disclose the measuring structure as applied to Claim 27 above.

Ohkawa does not disclose the measurement of capacitance of said device under test to determine the thickness of a gate oxide capacitor.

Mahant-Shetti discloses the measurement of capacitance of said device under test to determine the thickness of a gate oxide capacitor (column 5, lines 18-19).

Therefore, it would have been obvious to a person of ordinary skill in the art to measure the capacitance of said device under test to determine the thickness of a gate oxide, as taught by Mahant-Shetti, as the relationship between capacitance and thickness of the dielectric are well known in the art.

#### ***Allowable Subject Matter***

5. Claims 2-5, 9-12, 16-19, & 23-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art cited teaches various methods of testing capacitance of semiconductor structures; however, the prior art fails to teach the mathematical

computations and steps as taught by the applicant in the above mentioned claims.

### ***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Stein et al., US 6,541,986, discloses a method of measuring thickness, through the measurement of capacitance with the use of an oscillator. Fan et al., US 6,404,222, discloses a method of measuring capacitance of a semiconductor with the use of FET inverters and a signal generator. Froment, US 6,366,098, discloses a method of measuring capacitance and further calculating the dielectric thickness with the use of an FET inverter.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marina Kramskaya whose telephone number is (571)272-2146. The examiner can normally be reached on M-F 7:00-3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, N. Le can be reached on (571)272-2233. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MK

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PRIMARY EXAMINER

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